19-1856; Rev 2; 8/01

EVALUATION KIT AVAILABLE

10.7Gbps Laser Diode Drivers

General Description

The MAX3930/MAX3931/MAX3932 are designed for direct modulation of laser diodes at data rates up to 10.7Gbps. They provide adjustable laser bias and modulation currents and are implemented using Maxim's second-generation in-house SiGe process.

The MAX3930 accepts differential CML clock and data input signals and includes 50Ω on-chip termination resistors. It delivers a 1mA to 100mA laser bias current and a 20mA to 100mA modulation current with a typical (20% to 80%) 25ps rise time. An input data retiming latch can be used to reject input pattern-dependent jitter if a clock signal is available.

The MAX3931/MAX3932 have an alternate pad out with respect to the MAX3930. The MAX3931 includes the series damping resistor R_D on chip.

The MAX3930/MAX3931/MAX3932 also include an adjustable pulse-width control circuit to minimize laser pulse-width distortion.

Applications

SONET OC-192 and SDH STM-64 Transmission Systems

Up to 10.7Gbps Optical Transmitters

Section Regenerators

Features

- ♦ Single +5V or -5.2V Power Supply
- ♦ 108mA Supply Current
- ♦ Operates Up to 10.7Gbps
- ♦ 50Ω On-Chip Input Termination Resistors
- ♦ Programmable Modulation Current Up to 100mA
- ♦ Programmable Laser Bias Current Up to 100mA
- ♦ 25ps Rise Time (MAX3930/MAX3932)
- ♦ Adjustable Pulse-Width Control
- ♦ Selectable Data Retiming Latch
- ♦ ESD Protection
- ♦ Internal Series Damping Resistor (MAX3931)

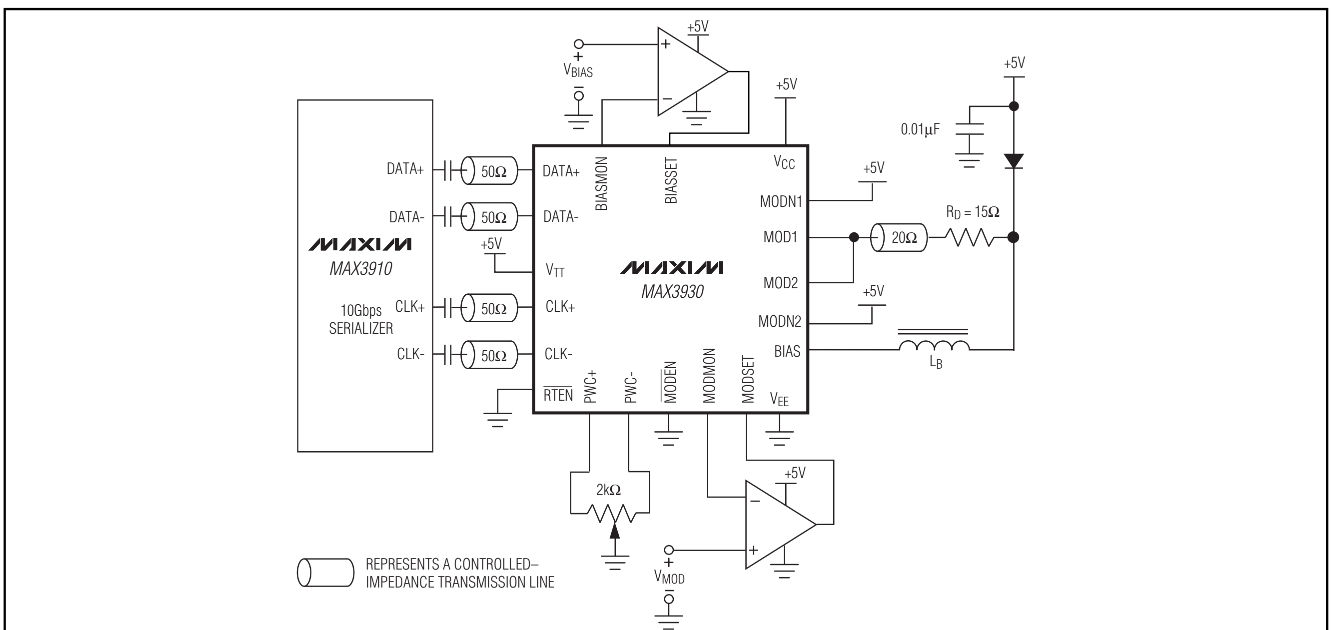
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3930E/D	-40°C to +85°C	Dice
MAX3931E/D	-40°C to +85°C	Dice
MAX3932E/D	-40°C to +85°C	Dice
MAX3932E/W	-40°C to +85°C	Wafer

Note: *Dice are designed to operate over a -40°C to +120°C junction temperature (T_J) range but are tested and guaranteed at T_A = +25°C.*

MAX3930/MAX3931/MAX3932†

Typical Application Circuit



† Covered by U.S. Patent number 5,883,910.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - V_{EE})..................................-0.5V to +6.0V
DATA+, DATA-, CLK+,
CLK- ....(V_{TT} - 1.2V) to the lower of (V_{TT} + 1.2V) or (V_{CC} + 0.5V)
$\overline{\text{MODEN}}$, $\overline{\text{RTEN}}$, V_{TT}, BIASMON, MODMON,
PWC+, and PWC- ....(V_{EE} - 0.5V) to (V_{CC} + 0.5V)
MODSET and BIASSET ....(V_{EE} - 0.5V) to (V_{EE} + 1.5V)
Storage Temperature Range ....-55°C to +150°C
Operating Junction Temperature ....-55°C to +150°C
Processing Temperature (die) ....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—MAX3930

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{EE} = +5V, I_{BIAS} = 50mA, I_{MOD} = 70mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{CC} - V_{EE}		+4.75	+5	+5.5	V
Power-Supply Current	I_{CC}	Excluding bias current and modulation current		108	140	mA
Single-Ended Input Resistance			42.5	50	57.5	Ω
Bias Current-Setting Range			1		100	mA
Bias Current-Setting Error		Bias current = 100mA, T_A = +25°C	-5		+5	%
		Bias current = 1mA, T_A = +25°C	-10		+10	
Bias Sensing Resistor	R_{BIAS}		2.7	3.0	3.3	Ω
Bias Current Temperature Stability		I_{BIAS} = 100mA (Note 1)	-480		+480	ppm/°C
		I_{BIAS} = 1mA (Note 1)		-200		
Bias Off-Current		BIASSET ≤ (V_{EE} + 0.4V)			0.05	mA
$\overline{\text{MODEN}}$ and $\overline{\text{RTEN}}$ Input High	V_{IH}		V_{EE} + 2.0			V
$\overline{\text{MODEN}}$ and $\overline{\text{RTEN}}$ Input Low	V_{IL}				V_{EE} + 0.8	V
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.75V to 5.5V (Note 2)	39.5	60		dB
SIGNAL INPUT FOR V_{TT} = V_{CC}						
Single-Ended Input (DC-Coupled)	V_{IS}	At high		V_{CC}		V
		At low	V_{CC} - 1		V_{CC} - 0.15	
Single-Ended Input (AC-Coupled)	V_{IS}	At high	V_{CC} + 0.075		V_{CC} + 0.4	V
		At low	V_{CC} - 0.4		V_{CC} - 0.075	
Differential Input Swing (DC-Coupled)	V_{ID}		0.3		2.0	Vp-p
Differential Input Swing (AC-Coupled)	V_{ID}		0.3		1.6	Vp-p
SIGNAL INPUT FOR V_{TT} = (V_{CC} - 1.3V)						
Input Common Mode	V_{ICM}			V_{CC} - 1.3		V

DC ELECTRICAL CHARACTERISTICS—MAX3930 (continued)

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{EE} = +5V, I_{BIAS} = 50mA, I_{MOD} = 70mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Input	V_{IS}	At high	V_{CC} - 1.225V		V_{CC} - 0.8	V
		At low	V_{CC} - 1.8		V_{CC} - 1.375	
Differential Input Swing	V_{ID}		0.3		2.0	Vp-p

DC ELECTRICAL CHARACTERISTICS—MAX3931/MAX3932

(V_{CC} - V_{EE} = 4.75V to 5.5V, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{EE} = +5V, I_{BIAS} = 50mA, I_{MOD} = 70mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{CC} - V_{EE}		+4.75	+5	+5.5	V
Power-Supply Current	I_{CC}	Excluding bias current and modulation current		108	140	mA
Single-Ended Input Resistance			42.5	50	57.5	Ω
Bias Current-Setting Range			1		100	mA
Bias Current-Setting Error		Bias current = 100mA, T_A = +25°C	-5		+5	%
		Bias current = 1mA, T_A = +25°C	-10		+10	
Bias Sensing Resistor	R_{BIAS}		2.7	3.0	3.3	Ω
Bias Current Temperature Stability		I_{BIAS} = 100mA (Note 1)	-480		+480	ppm/°C
		I_{BIAS} = 1mA (Note 1)		-200		
Bias Off-Current		BIASSET ≤ (V_{EE} + 0.4V)			0.05	mA
$\overline{\text{MODEN}}$ and $\overline{\text{RTEN}}$ Input High	V_{IH}		V_{EE} + 2.0			V
$\overline{\text{MODEN}}$ and $\overline{\text{RTEN}}$ Input Low	V_{IL}				V_{EE} + 0.8	V
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.75V to 5.5V (Note 2)	39.5	60		dB
SIGNAL INPUT FOR V_{TT} = V_{CC}						
Single-Ended Input (DC-Coupled)	V_{IS}	At high		V_{CC}		V
		At low	V_{CC} - 1		V_{CC} - 0.15	
Single-Ended Input (AC-Coupled)	V_{IS}	At high	V_{CC} + 0.075		V_{CC} + 0.4	V
		At low	V_{CC} - 0.4		V_{CC} - 0.075	
Differential Input Swing (DC-Coupled)	V_{ID}		0.3		2.0	Vp-p
Differential Input Swing (AC-Coupled)	V_{ID}		0.3		1.6	Vp-p

10.7Gbps Laser Diode Drivers

AC ELECTRICAL CHARACTERISTICS—MAX3930/MAX3932

(V_{CC} - V_{EE} = 4.75V to 5.5V, V_{TT} = V_{CC}, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{EE} = +5V, I_{MOD} = 70mA, and T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Data Rates		NRZ		10.7		Gbps
Modulation Current-Setting Range			20		100	mA
Modulation Current-Setting Error		20Ω load, T_A = +25°C	-5		+5	%
Modulation Sensing Resistor	R_{MOD}		2.7	3.0	3.3	Ω
Modulation Current Temperature Stability			-480		+480	ppm/°C
Modulation Off-Current		MODSET ≤ (V_{EE} + 0.4V)			0.1	mA
Output Current Rise Time	t_R	Z_L = 20Ω, 20% to 80% (Note 4)		25		ps
Output Current Fall Time	t_F	Z_L = 20Ω, 20% to 80% (Note 4)		29		ps
Setup/Hold Time	t_{SU}, t_{HD}	Figure 2		15		ps
Pulse-Width Adjustment Range		(Note 4)		±60		ps
Pulse-Width Stability		PWC+ and PWC- open (Note 4)		±0.3		ps
Pulse-Width Control Input Range		For PWC+ and PWC-	V_{EE} + 0	V_{EE} + 1.0	V_{EE} + 2.0	V
Overshoot		(Note 4)		11		%
Driver Random Jitter				0.75		ps_{RMS}
Driver Deterministic Jitter		(Note 5)		6.7		ps_{P-P}

AC ELECTRICAL CHARACTERISTICS—MAX3931

(V_{CC} - V_{EE} = 4.75V to 5.5V, V_{TT} = V_{CC}, T_A = -40°C to +85°C. Typical values are at V_{CC} - V_{EE} = +5V, I_{MOD} = 70mA, and T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Data Rates		NRZ		10.7		Gbps
Modulation Current-Setting Range			20		100	mA
Modulation Current-Setting Error		20Ω load, T_A = +25°C	-5		+5	%
Modulation Sensing Resistor	R_{MOD}		2.7	3.0	3.3	Ω
Output Series Resistance		R_{MOD1} in parallel with R_{MOD2}	12.75	15	17.25	Ω
Modulation Current Temperature Stability			-480		+480	ppm/°C
Modulation Off-Current		MODSET ≤ (V_{EE} + 0.4V)			0.1	mA
Setup/Hold Time	t_{SU}, t_{HD}	Figure 2		15		ps
Pulse-Width Adjustment Range		(Note 4)		±60		ps
Pulse-Width Stability		PWC+ and PWC- open (Note 4)		±0.3		ps
Pulse-Width Control Input Range		For PWC+ and PWC-	V_{EE} + 0	V_{EE} + 1.0	V_{EE} + 2.0	V

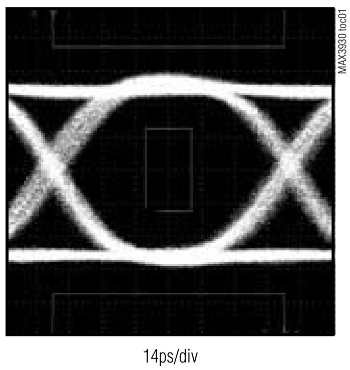
Note 1: Guaranteed by design and characterization.
Note 2: PSRR = 20 x log ($\Delta V_{CC}/(\Delta I_{MOD} \times 20\Omega)$). I_{MOD} = 100mA
Note 3: Guaranteed by design and characterization using the circuit shown in Figure 1.
Note 4: Measured using a 10.7Gbps repeating 0000 0000 1111 1111 pattern.
Note 5: Measured using a 10.7Gbps 2^{13}-1 PRBS with 80 zeros pattern.

Typical Operating Characteristics

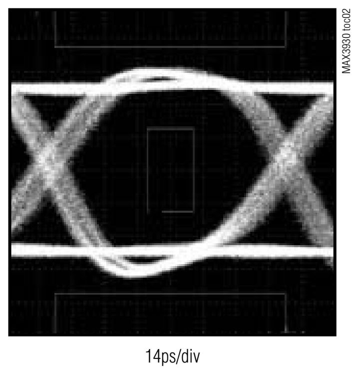
(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

MAX3930/MAX3932

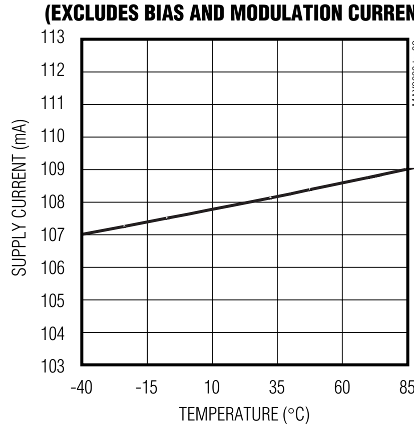
ELECTRICAL EYE DIAGRAM (I_{MOD} = 100mA, 2^{13}-1 +80 CID)



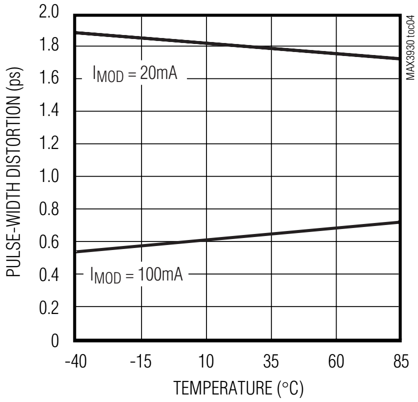
ELECTRICAL EYE DIAGRAM (I_{MOD} = 20mA, 2^{13}-1 +80 CID)



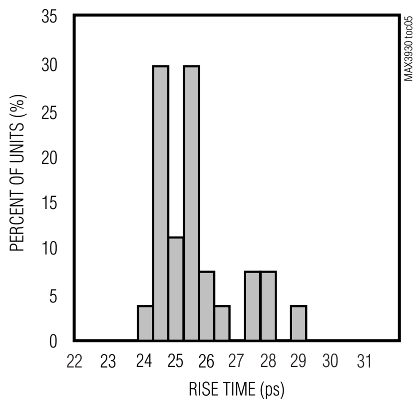
SUPPLY CURRENT vs. TEMPERATURE (EXCLUDES BIAS AND MODULATION CURRENTS)



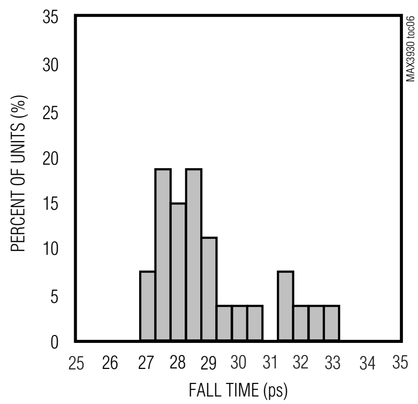
PULSE-WIDTH DISTORTION vs. TEMPERATURE



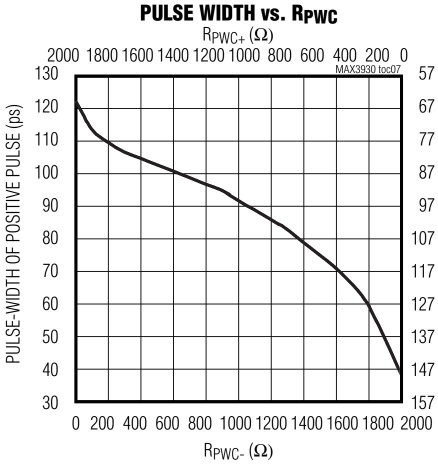
TYPICAL DISTRIBUTION OF RISE TIME



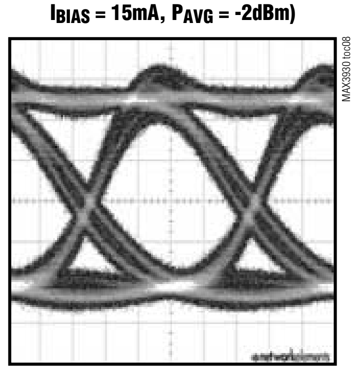
TYPICAL DISTRIBUTION OF FALL TIME



PULSE WIDTH vs. R_{PWC}

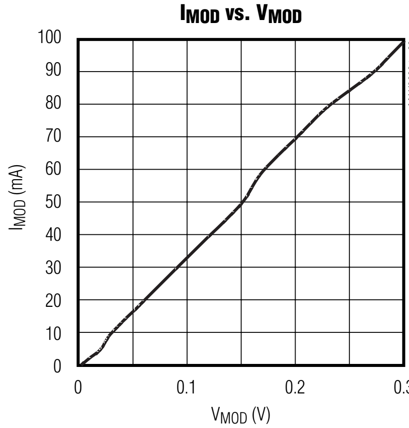


OC-192 OPTICAL EYE DIAGRAM (I_{MOD} = 70mAp-p, I_{BIAS} = 15mA, P_{AVG} = -2dBm)



OPTICAL EYE DIAGRAM COURTESY OF NETWORK ELEMENTS, INC. COPYRIGHT©2000 BY NETWORK ELEMENTS, INC. ALL RIGHTS RESERVED.

I_{MOD} vs. V_{MOD}

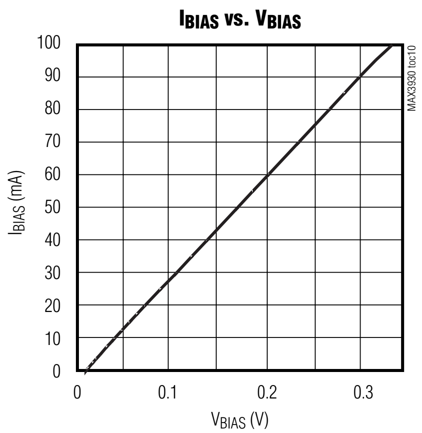


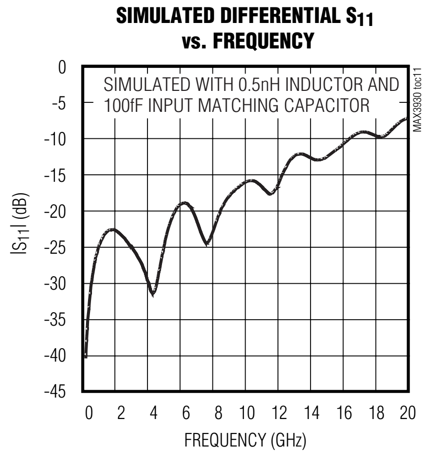
10.7Gbps Laser Diode Drivers

Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

MAX3930/MAX3932





Pad Description

MAX3930 PAD	MAX3931/ MAX3932 PAD	NAME	FUNCTION
1, 5, 9, 12, 22, 23, 28, 29	1, 3, 5, 7, 9, 10, 12, 22, 23, 28, 29	V_{CC}	Power-Supply Voltage (V_{CC} - V_{EE} = 5V). All pads must be connected to V_{CC}.
2	2	DATA+	Noninverting Data Input. CML with on-chip termination resistor.
3	—	V_{TT}	Terminating Voltage for Data Inputs
4	4	DATA-	Inverting Data Input. CML with on-chip termination resistor.
6	6	CLK+	Noninverting Clock Input for Data Retiming. CML with on-chip termination resistor.
7	—	V_{TT}	Terminating Voltage for Clock Inputs
8	8	CLK-	Inverting Clock Input for Data Retiming. CML with on-chip termination resistor.
10, 11, 17, 18, 21, 32, 35, 36, 37	11, 17, 18, 19, 32, 35, 36, 37	V_{EE}	Power-Supply Voltage (V_{CC} - V_{EE} = 5V)
13	13	$\overline{\text{RTEN}}$	TTL/CMOS Data Retiming Input. Low for latched data, high for direct data. Internal 100kΩ pullup to V_{CC}.
14	14	PWC+	Positive Input for Modulation Pulse-Width Adjustment. Connected to ground through R_{PWC}.
15	15	PWC-	Negative Input for Modulation Pulse-Width Adjustment. Connected to ground through R_{PWC}.
16	16	$\overline{\text{MODEN}}$	TTL/CMOS Modulation Enable Input. Low for normal operation, high to switch modulation output off. Internal 100kΩ pullup to V_{CC}.
19	20	MODMON	Modulation Current Monitor (V_{MODMON} - V_{EE}) / R_{MOD} = I_{MOD}
20	21	MODSET	Modulation Current Set. Connected to the output of the external operational amplifier (see *Design Procedure*).
24, 27	24, 27	MODN2, MODN1	Complementary Laser Modulation Current Outputs. Connect to V_{CC}.
25, 26	25, 26	MOD2, MOD1	Laser Modulation Current Outputs
30	30	BIAS	Laser Bias Current Output
31	31	N.C.	No Connection. Leave unconnected.
33	33	BIASSET	Bias Current Set. Connected to the output of the external operational amplifier (see *Design Procedure*).
34	34	BIASMON	Bias Current Monitor ($V_{BIASMON}$ - V_{EE}) / R_{BIAS} = I_{BIAS}

10.7Gbps Laser Diode Drivers

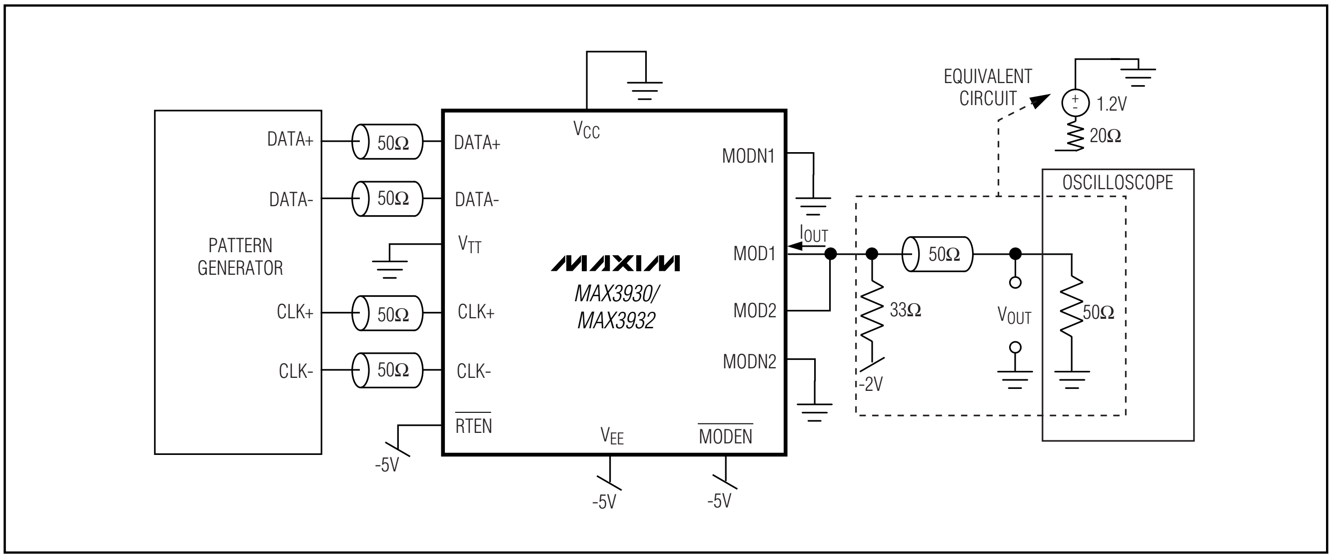


Figure 1. Test Circuit

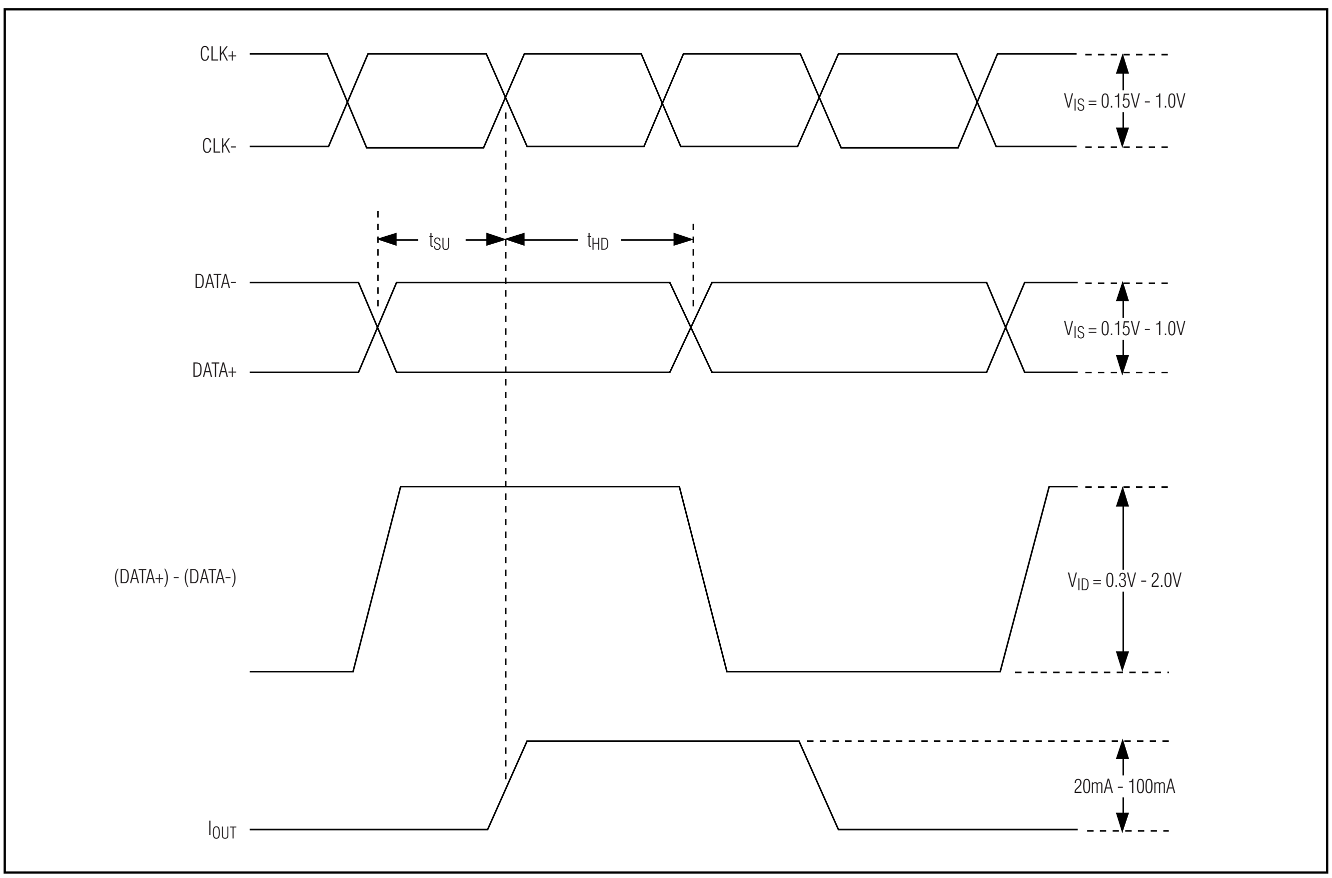


Figure 2. Required Input Signal, Setup/Hold-Time Definition, and Output Polarity

Detailed Description

The MAX3930 laser driver consists of two main parts, a high-speed modulation driver and a laser-biasing block. The circuit operates from a single +5V or -5.2V supply. When operating from a +5V supply, connect all V_{CC} pins to +5V and all V_{EE} pins to ground. If operating from a -5.2V supply, connect all V_{EE} pins to -5.2V and all V_{CC} pins to ground. To eliminate pattern-dependent jitter on the input data signal, the device accepts a differential CML clock signal for data retiming. When $\overline{RTEN}$ is tied to a low potential, the input data is synchronized by the clock signal. When $\overline{RTEN}$ is tied high or left floating, the input data is transmitted directly to the output stage (retiming is disabled).

The output stage is composed of a high-speed differential pair and a programmable modulation current source with a maximum modulation current of 100mA. The rise and fall times are typically 25ps and 29ps, respectively.

The MAX3930/MAX3932 modulation output is optimized for driving a 20Ω load. The minimum voltage required at MOD is 1.55V. To interface with a laser diode, a series damping resistor (R_D) is required for impedance matching (R_D = 15Ω, assuming a laser resistance of 5Ω; see *Typical Application Circuit*).

The MAX3931 output has an internal series damping resistor consisting of two parallel 30Ω resistors in series with the output. This simplifies interfacing with the laser diode. The MAX3931/MAX3932 have an alternate pad out with respect to MAX3930.

At the 10.7Gbps data rate, any capacitive load at the cathode of a laser diode will degrade the optical output performance. Since the BIAS output is directly connected to the laser cathode, minimize the parasitic capacitance associated with this pad by using a ferrite bead (L_B) to isolate the BIAS pin from the laser cathode.

Optional Input Data Retiming

To eliminate pattern-dependent jitter on the input data, a synchronous differential clock signal should be connected to the CLK+ and CLK- inputs, and the $\overline{RTEN}$ control input should be tied low. The input data is retimed on the rising edge of CLK+. If $\overline{RTEN}$ is tied high or left floating, the retiming function is disabled, and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

Modulation Output Enable

The MAX3930/MAX3931/MAX3932 incorporate a modulation current enable input. When $\overline{MODEN}$ is low, the modulation outputs (MOD1, MOD2) are enabled. When $\overline{MODEN}$ is high, the modulation outputs (MOD1, MOD2) are disabled. The typical laser enable time is 2ns, and the typical disable time is 5ns.

Pulse-Width Control

The pulse-width control circuit can be used to precompensate for laser pulse-width distortion. The differential voltage between PWC+ and PWC- adjusts the pulse-width compensation.

When PWC+ and PWC- are left open, the pulse-width control circuit is automatically disabled.

Current Monitors

The MAX3930/MAX3931/MAX3932 feature a bias current monitor output (BIASMON) and a modulation current monitor output (MODMON). The voltage at BIASMON is equal to ($I_{BIAS} \times R_{BIAS}$) + V_{EE}, and the voltage at MODMON is equal to ($I_{MOD} \times R_{MOD}$) + V_{EE}, where I_{BIAS} represents the laser bias current, I_{MOD} represents the modulation current, and R_{BIAS} and R_{MOD} are internal 3Ω (±10%) resistors. BIASMON and MODMON should be connected to the inverting input of an operational amplifier to program the bias and modulation current (see *Design Procedure*).

Design Procedure

When designing a laser transmitter, the optical output is usually expressed in terms of average power and extinction ratio. Table 1 gives relationships that are helpful in converting between the optical average power and the modulation current. These relationships are valid if the mark density and duty cycle of the optical waveform are 50%.

Programming the Modulation Current

For a desired laser average optical power, P_{AVG}, and optical extinction ratio, r_e, the required modulation current can be calculated based on the laser slope efficiency, η, using the equations in Table 1.

To program the desired modulation current, connect the inverting input of an operational amplifier (such as the MAX480) to MODMON and connect the output to MODSET. Connect the positive op amp voltage supply to V_{CC} and the negative supply to V_{EE} (for +5V operation, V_{CC} = +5V and V_{EE} = ground; for -5.2V operation, V_{CC} = ground and V_{EE} = -5.2V). The modulation current is set by connecting a reference voltage, V_{MOD}, to the noninverting input of the operational amplifier. Refer to the I_{MOD} vs. V_{MOD} graph in the *Typical Operating Characteristics* to select the value of V_{MOD} that corresponds to the required modulation current.

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P_0 + P_1) / 2$
Extinction Ratio	r_e	$r_e = P_1 / P_0$
Optical Power of a "1"	P_1	$P_1 = 2P_{AVG}\ r_e / (r_e + 1)$
Optical Power of a "0"	P_0	$P_0 = 2P_{AVG} / (r_e + 1)$
Optical Amplitude	P_{p-p}	$P_{p-p} = P_1 - P_0 = 2P_{AVG}(r_e - 1) / (r_e + 1)$
Laser Slope Efficiency	η	$\eta = P_{p-p} / I_{MOD}$
Modulation Current	I_{MOD}	$I_{MOD} = P_{p-p} / \eta$

Note: *Assuming a 50% average input duty cycle and mark density.*

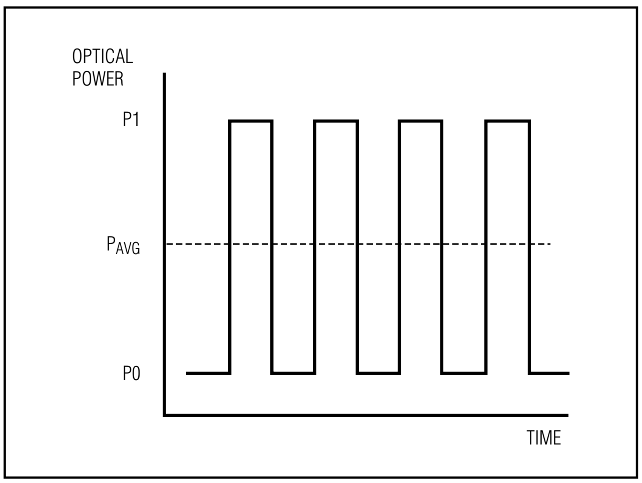


Figure 3. Optical Power Relations

Programming the Bias Current

To program the desired laser bias current, connect the inverting input of an operational amplifier (such as the MAX480) to BIASMON, and connect the output to BIASSET. Connect the positive op amp voltage supply to V_{CC} and the negative supply to V_{EE} (for +5V operation, V_{CC} = +5V and V_{EE} = ground; and for -5.2V operation, V_{CC} = ground and V_{EE} = -5.2V). The laser bias current is set by connecting a reference voltage, V_{BIAS}, to the noninverting input of the operational amplifier. Refer to the I_{BIAS} vs. V_{BIAS} graph in the *Typical Operating Characteristics* to select the value of V_{BIAS} that corresponds to the required laser bias current.

Interfacing with Laser Diodes

Refer to Maxim Application Note HFAN-2.0, *Interfacing Maxim Laser Drivers with Laser Diodes,* for detailed information.

To minimize optical output aberrations caused by signal reflections at the electrical interface to the laser diode, a series damping resistor (R_D) is required (Figure 4). The MAX3930/MAX3932 modulation outputs are optimized for a 20Ω load; therefore, the series combination of R_D and R_L (where R_L represents the laser diode resistance) should equal 20Ω. Typical values for R_D are 13Ω to 17Ω. The MAX3931 includes an on-chip series damping resistor R_D at 15Ω (Figure 5).

For best performance, a bypass capacitor (C), typically 0.01µF, should be placed as close as possible to the anode of the laser diode.

In some applications (depending on the laser diode parasitic inductance), an RF matching network at the laser cathode will improve the optical output.

Applications Information

Wire Bonding Die

For high current density and reliable operation, the MAX3930/MAX3931/MAX3932 use gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques. Do not use wedge bonding. Die-pad size is 3.0mils (76µm) and 4.5mils (114µm). Die thickness is 8mils (203µm). Die size is 46mils x 81mils (1.168mm x 2.057mm).

Layout Considerations

To minimize inductance, keep the connections between the driver output and the laser diode as short as possible. Optimize the laser diode performance by placing a bypass capacitor as close as possible to the laser anode. Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Use controlled impedance lines for the clock and data inputs.

Laser Safety and IEC 825

Using the MAX3930/MAX3931/MAX3932 laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Customers must determine the level of fault tolerance required by their application, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

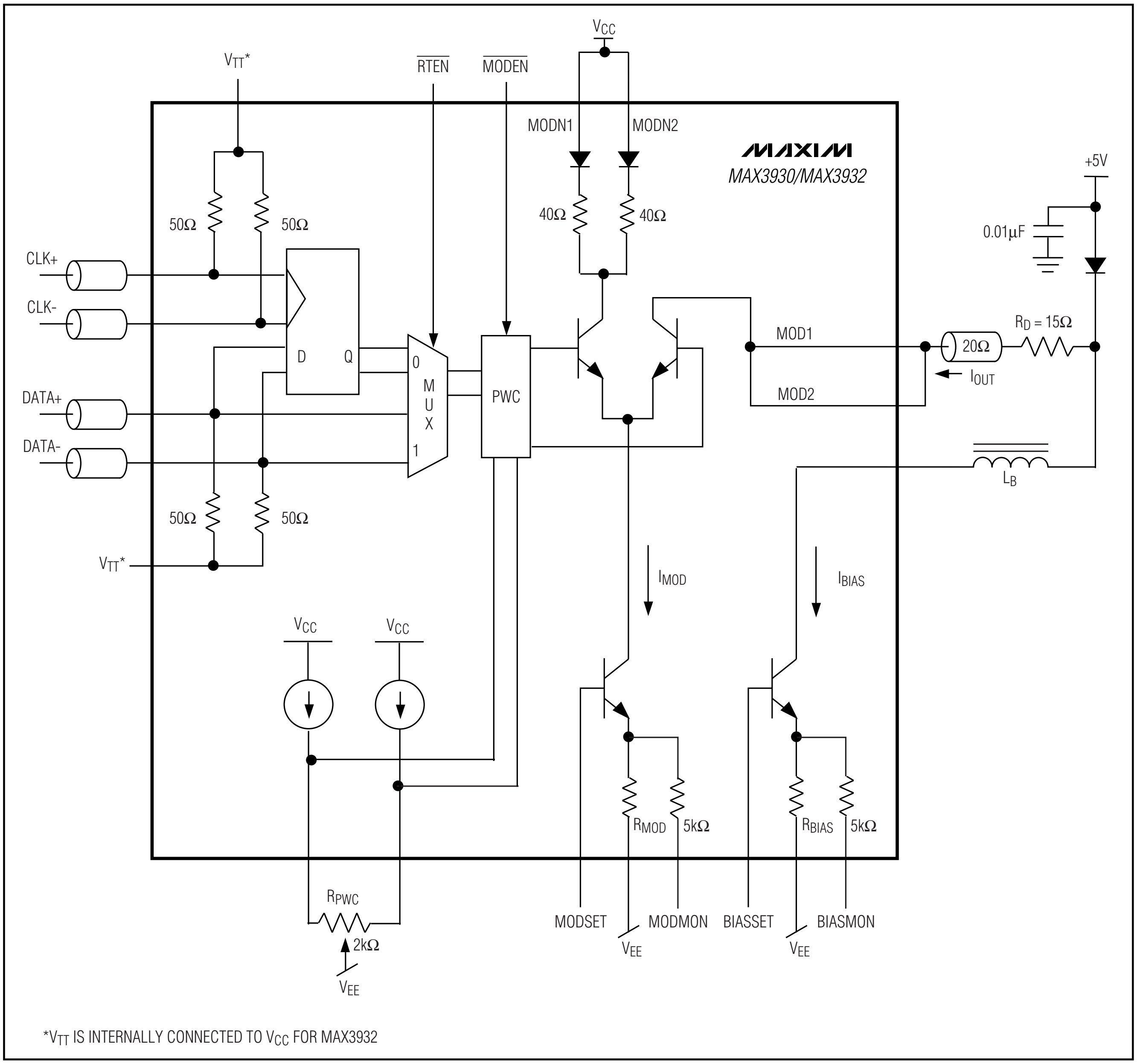


Figure 4. MAX3930/MAX3932 Functional Diagram

10.7Gbps Laser Diode Drivers

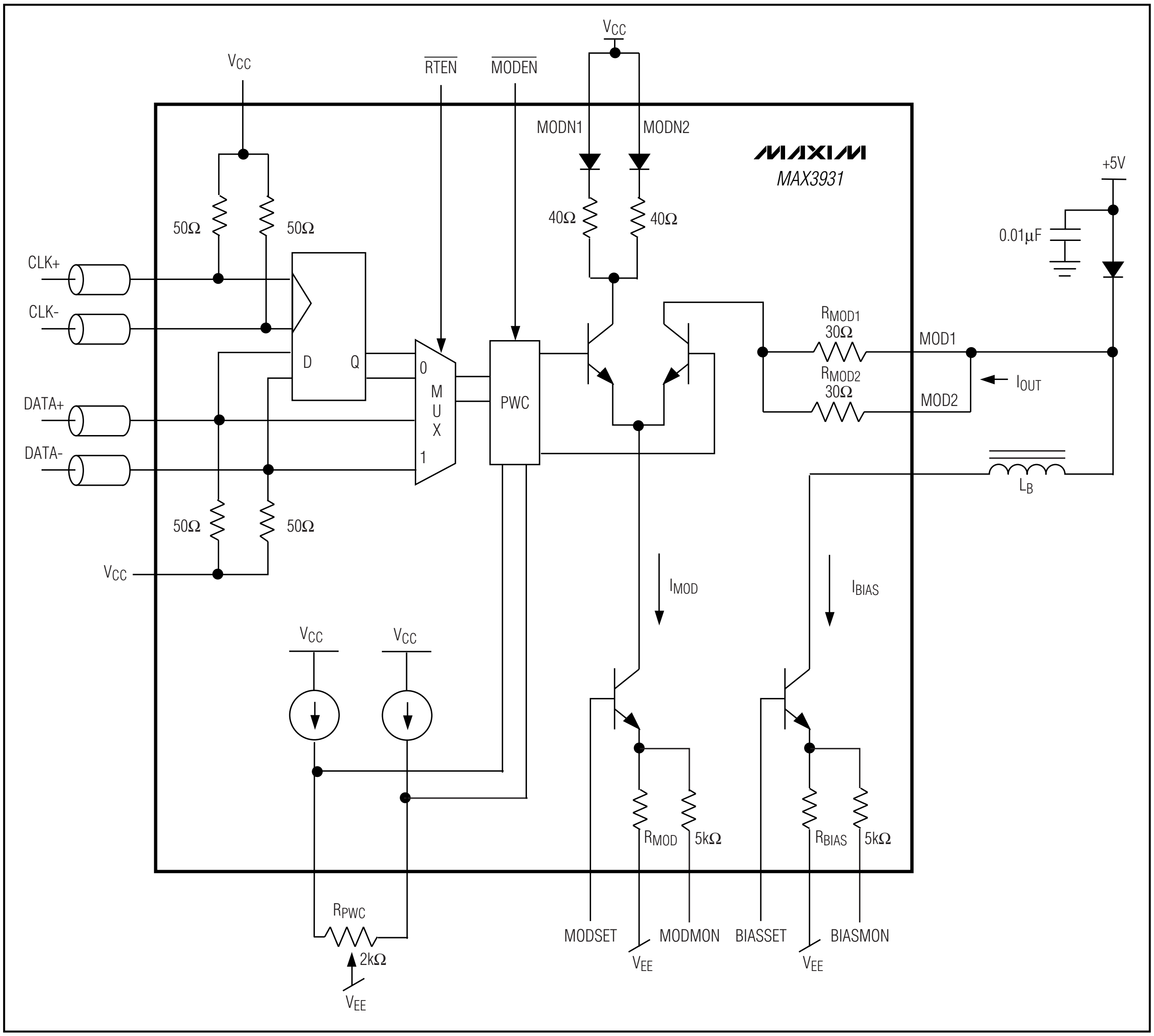


Figure 5. MAX3931 Functional Diagram

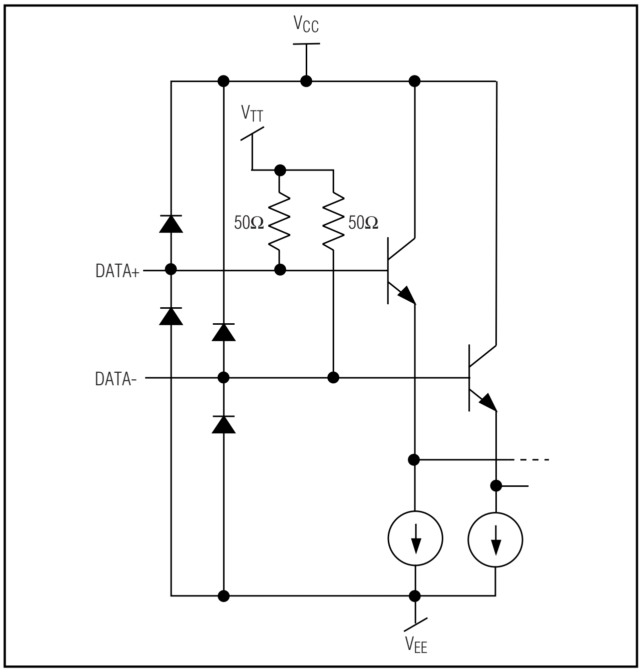


Figure 6. MAX3930 Equivalent Input Circuit

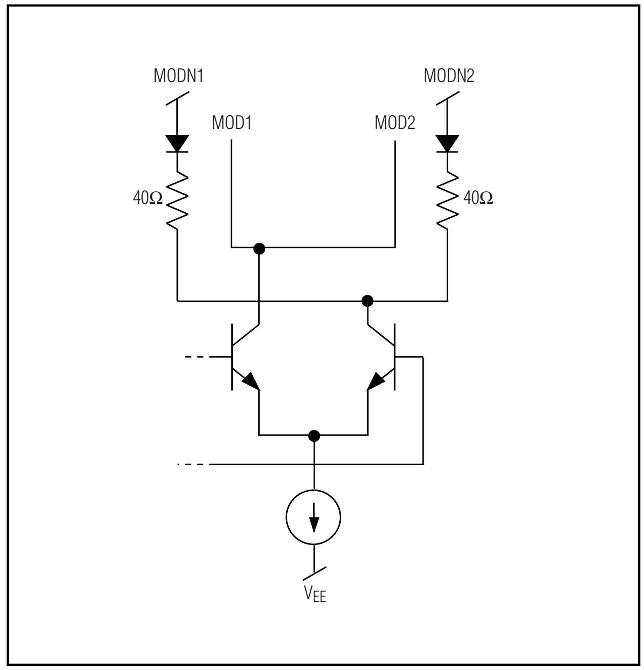


Figure 7. MAX3930/MAX3932 Equivalent Output Circuit

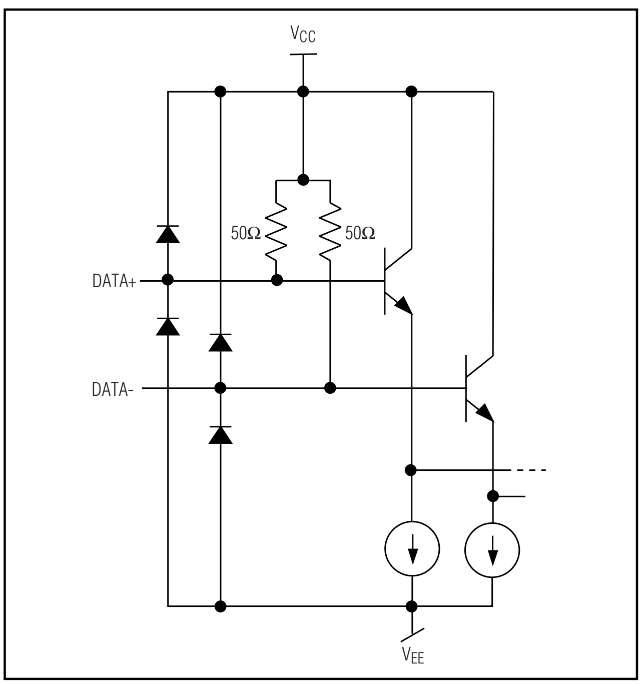


Figure 8. MAX3931/MAX3932 Equivalent Input Circuit

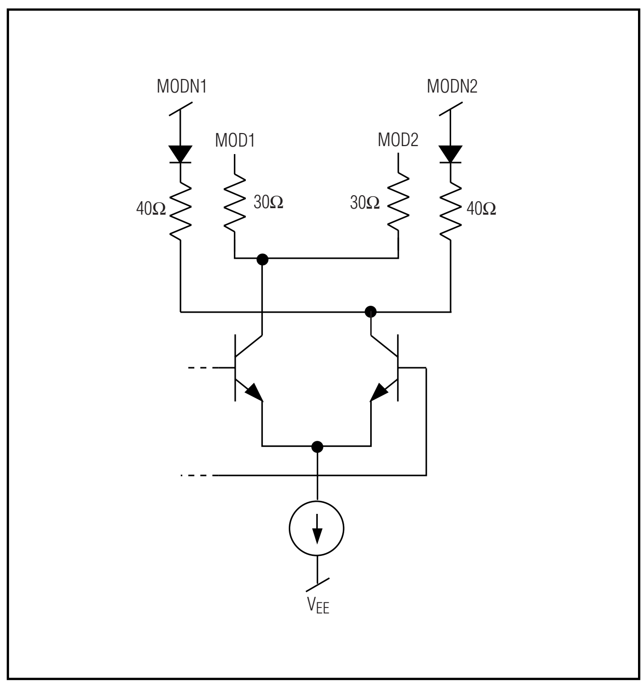
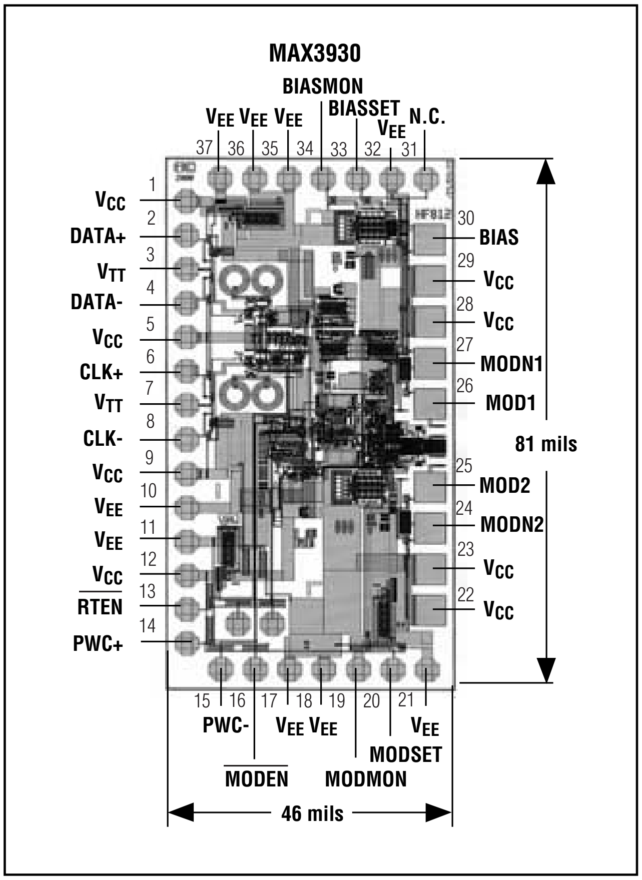
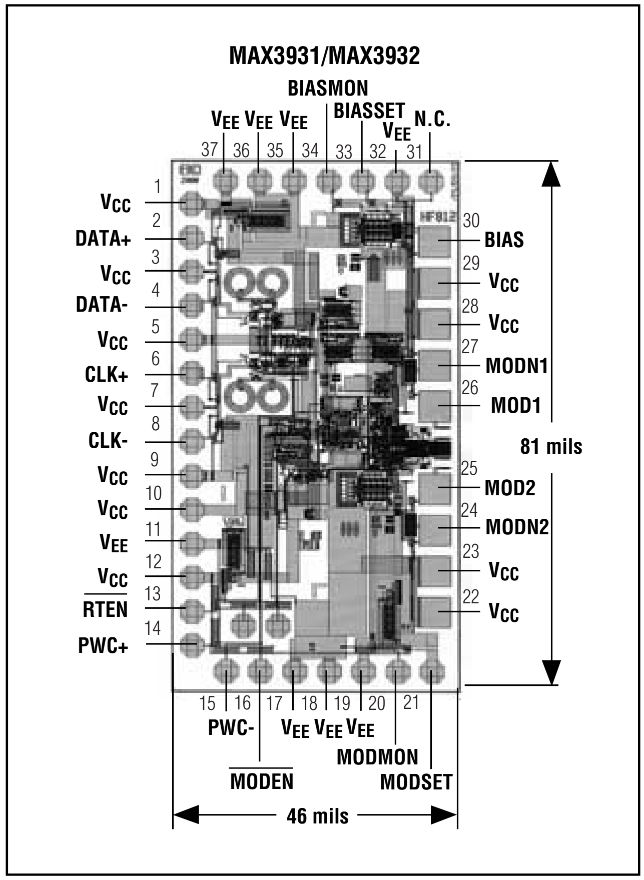


Figure 9. MAX3931 Equivalent Output Circuit

Chip Topography





Chip Information

TRANSISTOR COUNT: 1555

SUBSTRATE: SOI

PROCESS: BiPOLAR SILICON GERMANIUM

DIE THICKNESS: 8 mils